CLAIMS

1. (Original) A semiconductor device comprising:

(a) a pattern of conductive lines within a layer of the semiconductor device, wherein the conductive lines have a defined line width;

(b) dielectric surrounding the pattern of conductive lines in the layer; and

(c) a plurality of columnar gaps in the dielectric, which columnar gaps have an average feature dimension that is not greater than about 0.4 times the defined line width.

2. (Original) The semiconductor device of claim 1, wherein the layer of the semiconductor device is a metalization layer.

3. (Original) The semiconductor device of claim 1, wherein the conductive lines comprise copper.

4. (Original) The semiconductor device of claim 1, wherein the dielectric comprises a material selected from the group consisting of silicon oxide, silicon oxycarbide, fluorinated silicate glass, silicon nitride, spin-on organic materials, spin-on inorganic materials, and spin-on inorganic-hybrid materials.

5. (Original) The semiconductor device of claim 1, further comprising a layer deposited over the columnar gaps to enclose said gaps within the semiconductor device.

6. (New) The semiconductor device of claim 1, wherein the columnar gaps comprise periodically distributed gaps in the dielectric.

7. (New) The semiconductor device of claim 1, wherein the columnar gaps have a diameter of at most about 25 nanometers.

8. (New) The semiconductor device of claim 1, wherein the dielectric layer comprises a silicon containing material.

9. (New) The semiconductor device of claim 1, wherein the average feature dimension is between about 0.1 and about 0.35 times the defined line widths.